Preliminary

OKI Semiconductor

ML9060

1/2 DUTY, 160-OUTPUT STATIC LCD DRIVER

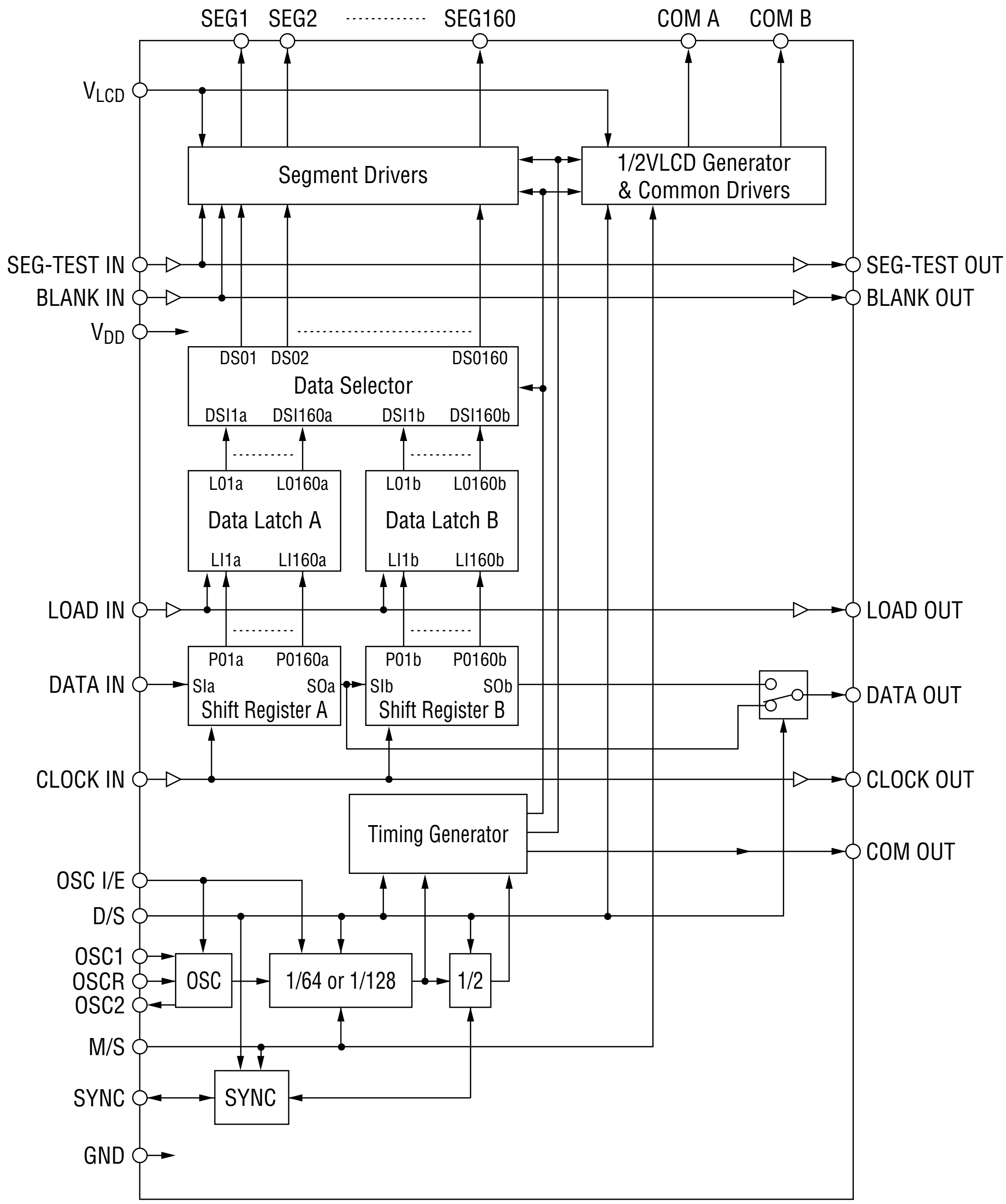
GENERAL DESCRIPTION

The ML9060 consists of a 320-bit shift register, a 320-bit data latch, 160 sets of LCD drivers, and a common signal generator circuit.
The LCD display data is input serially to the shift register from the DATA IN pin in synchronization with the CLOCK IN signal, and is stored in the data latch by the LOAD IN signal.
The LCD display data stored in the data latch is output via the LCD drivers.
A maximum of 160 segments of LCD can be driven in static display mode and a maximum of 320 segments can be driven directly in the 1/2 duty display mode.
It is possible to select the mode of using the internal oscillator circuit or the mode of using an external clock for the common signal generator circuit. The ML9060 also outputs the sync signal during the 1/2 duty display mode.

FEATURES

- Logic power supply : 2.7 to 5.5V
- LCD Driving voltage : 4.5 to 16V
- Maximum number of segments that can be driven:
  Static display mode : 160 segments
  1/2 Duty display mode : 320 segments
- Serial transfer clock : 1 MHz max.
- The microcontroller interface consists of the three signals DATA IN, CLOCK IN, and LOAD IN.
- An RC oscillator circuit is built in which can use either an external resistor or the internal resistor.
- Cascade connection of several ICs is possible.
- Built-in common signal generator circuit.
- Built-in common output mid-level voltage generator circuit.
- Input for turning all segments ON is available (SEG-TEST IN).
- Input for turning all segments OFF is available (BLANK IN).
- Gold bump chip Product name: ML9060DVWA

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Logic power supply voltage	V_{DD}	Ta = 25°C	–0.3 to +6.5	V
LCD Driving voltage	V_{LCD}	Ta = 25°C	0 to 18	V
Input voltage	V_I	Ta = 25°C	GND–0.3 to V_{DD}+0.3	V
Storage temperature	T_{STG}	—	–55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Range	Unit
Logic power supply voltage	V_{DD}*	—	2.7 to 5.5	V
LCD Driving voltage	V_{LCD}*	—	4.5 to 16	V
Operating temperature	T_{op}	—	–40 to +85	°C

*: Use with $V_{DD} \leq V_{LCD}$

Note: Never place a short between an output pin and another output pin or between an output pin and other pins (input pins, I/O pins, or power supply pins).

ELECTRICAL CHARACTERISTICS

DC Characteristics

(V_{DD} = 2.7 to 5.5V, V_{LCD} = 4.5 to 16V, Ta = –40 to +85°C)

Parameter		Symbol	Condition	Min.	Typ.	Max.	Unit	Applicable pin
"H" Input voltage		V_{IH1} *1	—	$0.7V_{DD}$	—	V_{DD}	V	DATA IN CLOCK IN LOAD IN SEG-TEST IN BLANK IN M/S, D/S OSC1, OSC I/E
		V_{IH2} *2		$0.8V_{DD}$	—	V_{DD}		
"L" Input voltage		V_{IL1} *1	—	GND	—	$0.3V_{DD}$	V	
		V_{IL2} *2		GND	—	$0.2V_{DD}$		
Input leakage current 1		I_{L1}	$V_I = V_{DD}$ or 0V	—	—	±1.0	µA	
Input leakage current 2		I_{L2}	$V_I = V_{DD}$ or 0V D/S = "H" M/S = "L"	—	—	±10	µA	SYNC
"H" Output voltage	Segment	V_{OHS}	$I_O = -30\mu A$	$V_{LCD}-0.2$	—	—	V	SEG1 to SEG160
	Common	V_{OHC} *3	$I_O = -150\mu A$	$V_{LCD}-0.2$	—	—	V	COM A, COM B
	Logic	V_{OHL1}	$I_O = -100\mu A$	$0.9V_{DD}$	—	—	V	DATA OUT CLOCK OUT LOAD OUT SEG-TEST OUT BLANK OUT COM OUT SYNC
		V_{OHL2}	$I_O = -200\mu A$	$0.9V_{DD}$	—	—	V	OSC2
"M" Output voltage	Common	V_{OMC} *3	$I_O = \pm 150\mu A$	$1/2V_{LCD}$ -0.15	$1/2V_{LCD}$	$1/2V_{LCD}$ $+0.15$	V	COM A, COM B
"L" Output voltage	Segment	V_{OLS}	$I_O = 30\mu A$	—	—	0.2	V	SEG1 to SEG160
	Common	V_{OLC} *3	$I_O = 150\mu A$	—	—	0.2	V	COM A, COM B
	Logic	V_{OLL1}	$I_O = 100\mu A$	—	—	$0.1V_{DD}$	V	DATA OUT CLOCK OUT LOAD OUT SEG-TEST OUT BLANK OUT COM OUT SYNC
		V_{OLL2}	$I_O = 200\mu A$	—	—	$0.1V_{DD}$	V	OSC2
Output resistance	Segment	R_{SEG}		—	—	10	kΩ	SEG1 to SEG160
	Common	R_{COM}		—	—	1.5	kΩ	COM A, COM B

"M": Middle level

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Applicable pin
Static supply current *4	I_{DDS1}	D/S = "L" (Static) Fix other input levels at either "H" or "L" Oscillator stopped No load	—	—	TBD	μA	V_{DD}
	I_{DDS2}	D/S = "H" (1/2duty) Fix other input levels at either "H" or "L" Oscillator stopped No load	—	—	TBD	μA	V_{DD}
	I_{LCDS1}	D/S = "L" (Static) Fix other input levels at either "H" or "L" Oscillator stopped No load	—	—	TBD	μA	V_{LCD}
	I_{LCDS2}	D/S = "H" (1/2duty) Fix other input levels at either "H" or "L" Oscillator stopped No load	—	—	TBD	μA	V_{LCD}
Dynamic supply current *4	I_{DD1}	V_{DD} = 5.5V D/S = "L" (Static) OSC1 is Open OSC2 is connected to OSCR Other inputs are "H" or "L" No load	—	—	TBD	mA	V_{DD}
	I_{DD2}	V_{DD} = 5.5V D/S = "H" (1/2duty) OSC1 is Open OSC2 is connected to OSCR Other inputs are "H" or "L" No load	—	—	TBD	mA	V_{DD}
	I_{LCD1}	V_{DD} = 5.5V D/S = "L" (Static) OSC1 is Open OSC2 is connected to OSCR Other inputs are "H" or "L" No load	—	—	TBD	μA	V_{LCD}
	I_{LCD2}	V_{DD} = 5.5V D/S = "H" (1/2duty) OSC1 is Open OSC2 is connected to OSCR Other inputs are "H" or "L" No load	—	—	TBD	μA	V_{LCD}

*1: Applicable to the DATA IN, LOAD IN, SEG-TEST IN, M/S, D/S, and OSC I/E pins.
*2: Applicable to the CLOCK IN, OSC1, and BLANK IN pins.
*3: Applicable to the voltage drop when the current flows into or out of one COM pin.
*4: The power supply current consumption will be determined finally at the end of sample evaluations.
The LCD display data of “0” and “1” are input alternately.

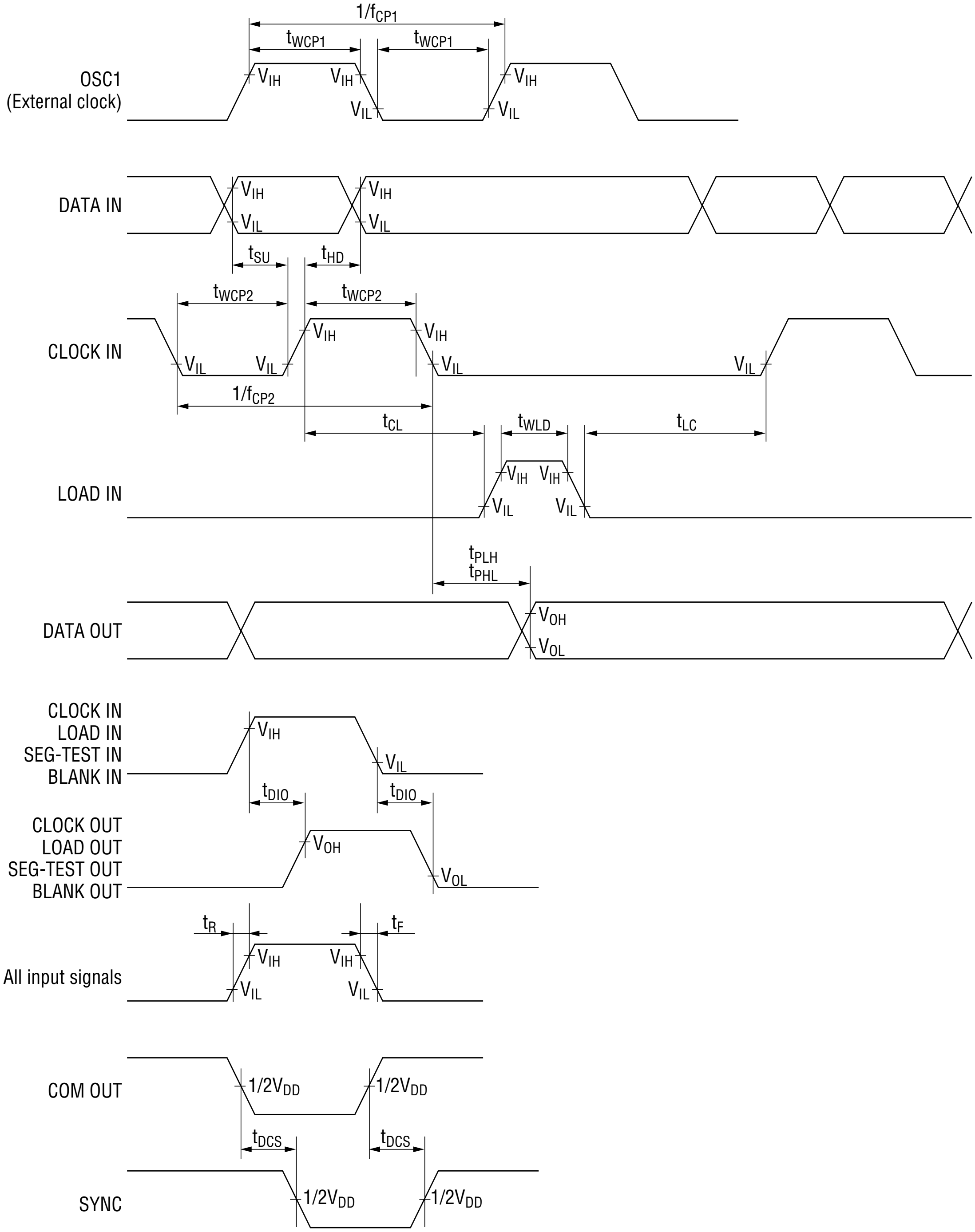
Switching Characteristics

(V_{DD} = 2.7 to 5.5V, V_{LCD} = 4.5 to 16V, Ta = –40 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Applicable pin
OSC IN Clock frequency (external input)	f_{CP1}	The clock is input to the OSC1 pin. The pins OSC2 and OSCR are left open. OSC I/E = "L"	—	—	25.6	kHz	OSC1
Clock pulse width (external input)	t_{WCP1}		50	—	—	μs	OSC1
External Rf clock frequency (internal oscillations)	f_{OSC1}	An Rf of 120k Ω ±2% is connected between OSC1 and OSC2. OSCR is left open. OSC I/E = 'H"	7.7	12.8	20.5	kHz	OSC1, OSC2
Internal Rf clock frequency (with the built-in oscillator)	f_{OSC2}	OSC1 open. OSC2 and OSCR shorted. OSC I/E tied to V_{DD} or any "H" level.	7.7	12.8	20.5	kHz	OSC1, OSCR, OSC2
Data clock frequency	f_{CP2}		—	—	1	MHz	CLOCK IN
Data clock pulse width	t_{WCP2}		100	—	—	ns	CLOCK IN
Data setup time	t_{SU}		50	—	—	ns	DATA IN
Data hold time	t_{HD}		50	—	—	ns	CLOCK IN
CLOCK to LOAD Period	t_{CL}		100	—	—	ns	CLOCK IN
LOAD to CLOCK Period	t_{LC}		100	—	—	ns	LOAD IN
LOAD Pulse width	t_{WLD}		100	—	—	ns	LOAD IN
CLOCK IN to DATA OUT delay time	t_{PLH} t_{PHL}	C_L=15pF	—	—	50	ns	CLOCK IN DATA OUT
IN to OUT delay time	t_{DIO}	No load	—	—	20	ns	CLOCK IN/OUT LOAD IN/OUT SEG-TEST IN/OUT BLANK IN/OUT
COM OUT to SYNC delay time	t_{DCS}	C_L=15pF	—	—	40	ns	COM OUT SYNC
Input signal rise time	t_R		—	—	50	ns	All inputs other than the OSCR input
Input signal fall time	t_F		—	—	50	ns	

* : The specifications of the internal Rf clock frequency and the external Rf clock frequency will be determined finally at the end of sample evaluations.

TIMING DIAGRAM



FUNCTIONAL DESCRIPTION

The ML9060 is an LCD driver LSI with an internal shift register and a set of internal data latches and is capable of driving LCD displays of up to 320 segments either in the static mode or in the 1/2 duty mode. The display data is read into the shift register serially from the DATA IN pin at the rising edge of the CLOCK IN input signal. The display data is transferred internally to the data latches at the High level of the LOAD IN input signal and is output to the segments via the segment drivers in this IC. The display data in the shift register is output via the DATA OUT pin in synchronization with the falling edge of the CLOCK IN input signal. The display data should be input in the sequence of SEG160, SEG159, ... , SEG2, SEG1 for proper display of data.

Description of Pin Functions

• M/S

This is the input pin for selecting either the Master mode or the Slave mode. This LSI goes into the master mode when this pin is High and enters the Slave mode when this pin is Low.

• D/S

This input pin is for selecting either the dynamic display mode at 1/2 duty (D mode - “H” input) or the static display mode (S mode - “L” input).
Note that the internal bias resistor is made ON in the dynamic (D) mode and is turned OFF in the static mode (S).

• OSC I/E

This is the input pin for selecting whether to use the external clock input mode, or the internal Rf oscillation mode or the external Rf oscillation mode.
When this pin is tied to the “H” level, the internal Rf oscillation mode or the external Rf oscillation is used. When this pin is tied to the “L” level, the external clock input is used for the operation of the LSI.
In the slave mode of operation of this LSI, any input to this pin will be ignored. Hence, tie this pin to V_{DD} or GND in the slave mode.

• OSC1, OSCR, OSC2

These are the pins for the oscillator for generating the common signal.

In the Master mode (M/S pin = “H”):

It is possible to select from among the three modes - internal Rf oscillation mode, external Rf oscillation mode, and the external clock input mode. During the static display operation mode, a common signal with 1/128th the frequency of the clock oscillator is output via the COM OUT pin.
During the 1/2 duty dynamic display operation mode, a common signal with 1/64th the frequency of the clock oscillator is output via the COM OUT pin.

- Internal Rf oscillation mode: Tie the OSC I/E pin to “H”, short the pins OSCR and OSC2, and leave the pin OSC1 open.
- External Rf oscillation mode: Tie the OSC I/E pin to “L”, connect an external resistor Rf between the pins OSC1 and OSC2, and leave the pin OSCR open.
- External clock input mode: Tie the OSC I/E pin to “L”, leave open the pins OSCR and OSC2, and input the external clock signal to the pin OSC1.

In the Slave mode (M/S pin = "L"):
Leave open the pins OSCR and OSC2 and connect the pin OSC1 to the COM OUT pin of the ML9060 which has been set in the master mode. The common signal that is input to the pin OSC1 will be used as the internal common signal and is also output via a buffer from the COM OUT pin.

• COM OUT
This is the common signal output pin. Connect this pin to the OSC1 pin of the ML9060 that is set in the slave mode.
During operation in the master mode (M/S pin = "H") for static display, a common signal with 1/128th the frequency of the oscillator is output.
During operation in the master mode (M/S pin = "H") for 1/2 duty dynamic display, a common signal with 1/64th the frequency of the oscillator is output.
During operation in the slave mode (M/S pin = "L"), the common signal that is input at the pin OSC1 is output from this pin via a buffer.

• SYNC
This is the I/O pin for common signal synchronization.
This pin becomes the synchronization signal output pin during operation in the master mode (M/S pin = "H") for 1/2 duty dynamic display.
This pin becomes the synchronization signal input pin during operation in the slave mode (M/S pin = "H") for 1/2 duty dynamic display.
For cascade operation in the 1/2 duty display mode, connect the SYNC pins of all ML9060 ICs used together.
During operation in the static display mode, this pin is tied to the "L" level inside the IC. Connect this pin either to GND or leave it open.

• DATA IN
This is the display data input pin. Input the display data in the sequence of SEG160, SEG159, ... , SEG2, SEG1. The segment is turned ON when the display data is "H" and OFF when "L".

• DATA OUT
This is the display data output pin. During the static display mode of operation, the data of the 160th stage of the shift register is output from this pin. During the 1/2 duty dynamic display mode, the data of the 320th stage of the shift register is output from this pin.

• CLOCK IN
This is the input pin for the shift clock of the display data. The display data that is input at the DATA IN pin is input serially to the shift register at the rising edge of the CLOCK IN signal. Also, the display data in the shift register is output from the DATA OUT pin at the falling edge of the CLOCK IN signal.

• CLOCK OUT
This is the output pin for the shift clock of the display data. The shift clock signal that is input to the CLOCK IN pin is output via a buffer from this pin.

• LOAD IN
This is the input pin for the display data load signal.
The display data in the shift register is output as such to the segment driver when this signal is at the "H" level. When this signal is made "L", the shift register is isolated from the segment drivers, and the display data of the shift register just before this pin goes "L" is retained in the data latches and transfered to the segment drivers.

• LOAD OUT
This is the output pin for the display data load signal. The load signal that is input to the LOAD IN pin is output from this pin via a buffer.

• SEG-TEST IN
This is the input pin for making all segments ON. When this pin is “H”, all segment outputs (SEG1 to SEG160) become ON irrespective of the display data and the Blank signal. When this pin is made “L”, each of the segment outputs (SEG1 to SEG160) become ON or OFF according to the display data.

• SEG-TEST OUT
This is the output pin for making all segments ON. The segment ON signal that is input to at the SEG-TEST IN pin is output via a buffer.

• BLANK IN
This is the input pin for making all segments OFF. When this pin is “H”, all segment outputs (SEG1 to SEG160) become OFF irrespective of the display data. When this pin is made “L”, each of the segment outputs (SEG1 to SEG160) becomes ON or OFF according to the display data. The BLANK IN is valid when the segment ON signal is "L".

• BLANK OUT
This is the output pin for making all segments OFF. The segment OFF signal that is input to the BLANK IN pin is output via a buffer.

• SEG1 to SEG160
These are the signal outputs for driving the LCD segments and are connected to the corresponding segment pins of the LCD panel.

During the Static mode of operation:
The SEGn output corresponds to bit n of the display data in the data latch A. The display data in the data latch B becomes invalid. In the segment ON condition, a signal with a phase opposite to that of the COM OUT signal is output from these pins. In the segment OFF condition, a signal with a phase identical to that of the COM OUT signal is output from these pins.

During the 1/2 duty dynamic display mode of operation:
The SEGn output corresponds to bit n of the display data in the data latch A when COM A has been selected and to bin n of the display data in the data latch B when COM B has been selected. In the segment display ON condition, a signal opposite in phase to that of the selected COM output is output from these pins. In the segment display OFF condition, a signal identical in phase to that of the selected COM output is output from these pins.

• COM A, COM B
These are the outputs for LCD display and are connected to the common pins of the LCD panel.

During the Static mode of operation:
COM A and COM B both output a signal with the same phase as that of the COM OUT signal.

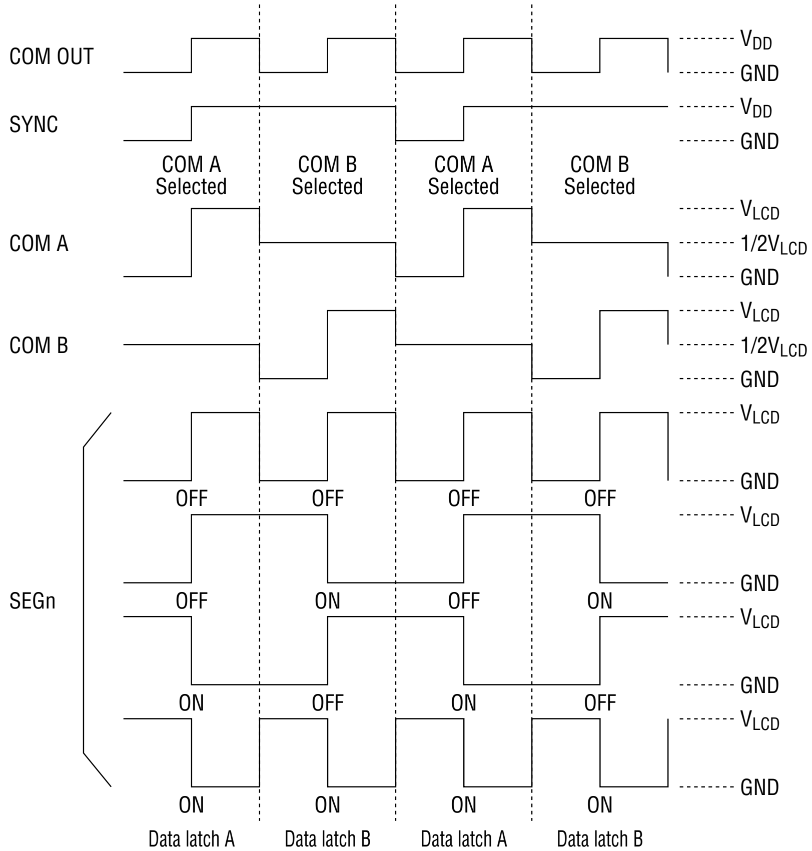
During the 1/2 duty dynamic display mode of operation:
COM A and COM B change their states at every cycle of the COM OUT signal and repeat the selected and non-selected modes always opposing each other in phase. A signal with the same phase as that of the COM OUT signal is output in the selected mode. A voltage equal to $1/2V_{LCD}$ is output in the non-selected mode.
When COM A is in the selected mode (that is, COM B is in the non-selected mode), the segment outputs (SEG1 to SEG160) output signals corresponding to the display data in the data latch A.
When COM B is in the selected mode (that is, COM A is in the non-selected mode), the segment outputs (SEG1 to SEG160) output signals corresponding to the display data in the data latch B.

• V_{DD}
This is the power supply input pin for the logic circuits.

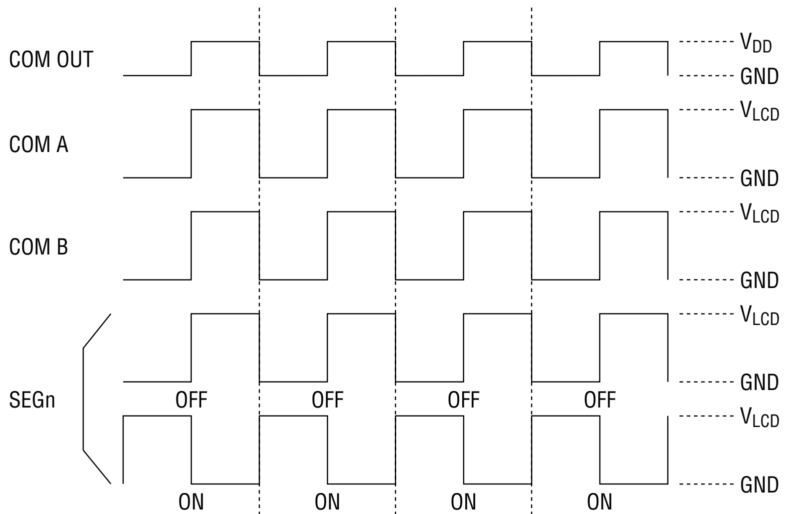
• V_{LCD}
This is the power supply input pin for the LCD drivers.

• GND
This is the ground pin for all circuits.

Segment Output and Common Output Waveforms
During the 1/2 duty display operation mode:

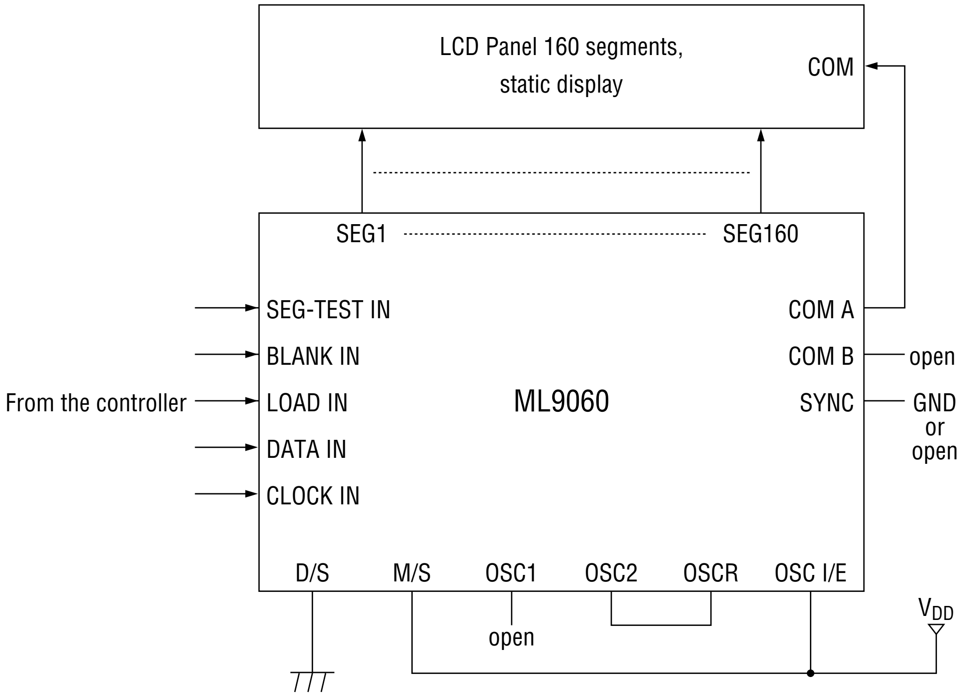


During the static display operation mode:

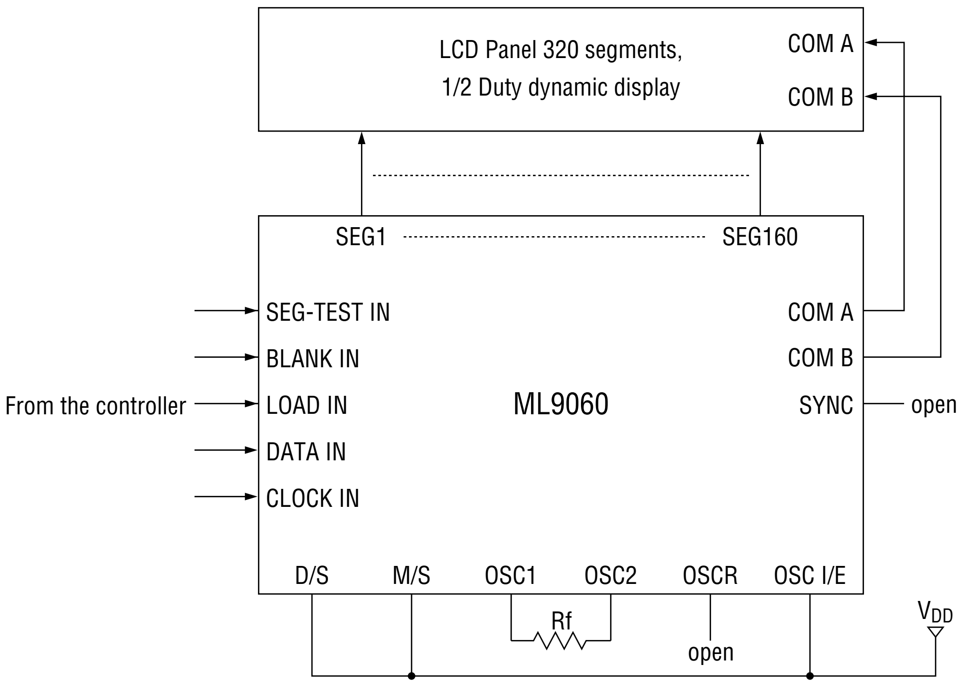


APPLICATION CIRCUIT EXAMPLES

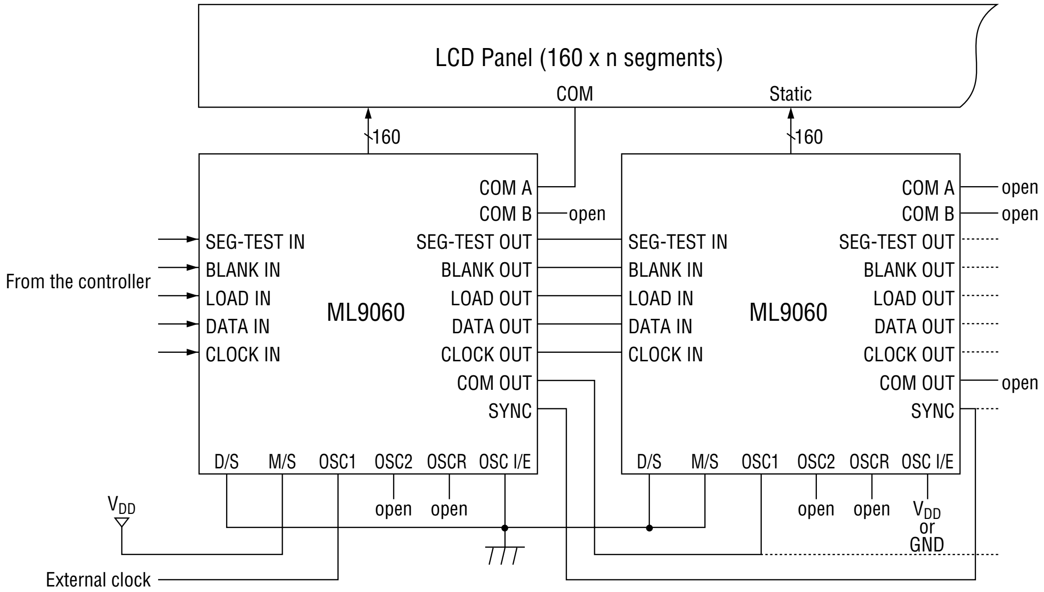
When a single ML9060 is used - Static display mode (internal Rf oscillation mode)



When a single ML9060 is used - 1/2 duty dynamic display mode (external Rf oscillation mode)

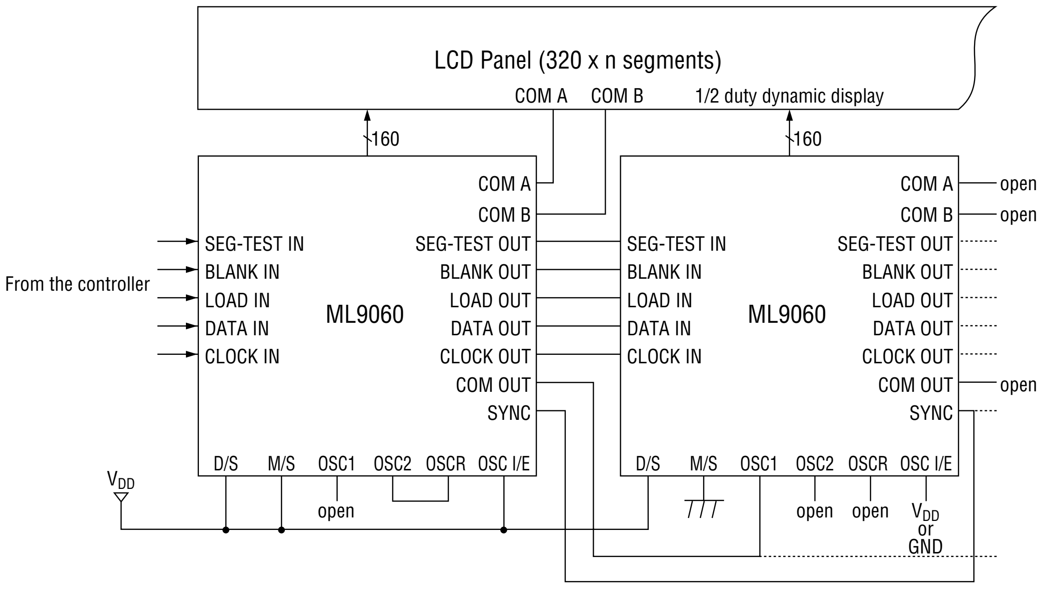


Cascade Connection - Static display mode (external clock input mode)



Note: Take care about the resistance and capacitance of wiring for cascade connection.

Cascade Connection - 1/2 duty dynamic display mode (internal Rf oscillation mode)

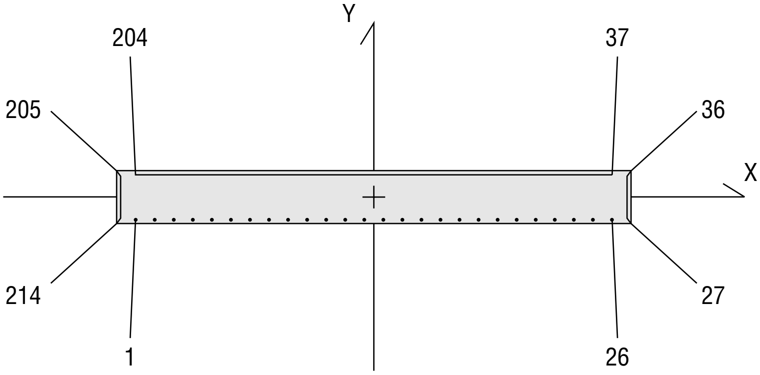


Note: Take care about the resistance and capacitance of wiring for cascade connection.

PAD CONFIGURATION

Pad layout (Pattern side)

Chip size : 14.50 × 1.48mm
Chip thickness : 625μm ± 30μm
Minimum bump pitch : 80μm
Bump size : 50 × 80μm
Bump height : 15μm ± 5μm
Bump height inside the chip : max. – min. ≤ 4μm
Bump hardness : max. 100 (HV: 25 g LOAD)



* : The substrate of the chip should either be connected to the GND level or be left open.

Pad Coordinates

Pad No.	Pad name	X-coordinate (μm)	Y-coordinate (μm)	Pad No.	Pad name	X-coordinate (μm)	Y-coordinate (μm)
1	NC	–6680	–561	21	OSC2	4008	–561
2	NC	–6146	–561	22	OSCR	4542	–561
3	SYNC	–5611	–561	23	OSC1	5077	–561
4	NC	–5077	–561	24	NC	5611	–561
5	COMOUT	–4542	–561	25	NC	6146	–561
6	NC	–4008	–561	26	NC	6680	–561
7	V_{LCD}	–3474	–561	27	NC	7121	–360
8	V_{LCD}	–2939	–561	28	NC	7121	–280
9	V_{LCD}	–2405	–561	29	DATA IN	7121	–200
10	NC	–1870	–561	30	NC	7121	–120
11	GND	–1336	–561	31	CLOCK IN	7121	–40
12	GND	–802	–561	32	LOAD IN	7121	40
13	GND	–267	–561	33	SEG-TEST IN	7121	120
14	D/S	267	–561	34	BLANK IN	7121	200
15	OSC I/E	802	–561	35	NC	7121	280
16	M/S	1336	–561	36	NC	7121	360
17	V_{DD}	1870	–561	37	NC	6680	561
18	V_{DD}	2405	–561	38	NC	6600	561
19	V_{DD}	2939	–561	39	NC	6520	561
20	NC	3474	–561	40	COMA	6440	561

NC: No Connection

Pad No.	Pad name	X-coordinate (μm)	Y-coordinate (μm)
41	COM B	6360	561
42	SEG1	6280	561
43	SEG2	6200	561
44	SEG3	6120	561
45	SEG4	6040	561
46	SEG5	5960	561
47	SEG6	5880	561
48	SEG7	5800	561
49	SEG8	5720	561
50	SEG9	5640	561
51	SEG10	5560	561
52	SEG11	5480	561
53	SEG12	5400	561
54	SEG13	5320	561
55	SEG14	5240	561
56	SEG15	5160	561
57	SEG16	5080	561
58	SEG17	5000	561
59	SEG18	4920	561
60	SEG19	4840	561
61	SEG20	4760	561
62	SEG21	4680	561
63	SEG22	4600	561
64	SEG23	4520	561
65	SEG24	4440	561
66	SEG25	4360	561
67	SEG26	4280	561
68	SEG27	4200	561
69	SEG28	4120	561
70	SEG29	4040	561
71	SEG30	3960	561
72	SEG31	3880	561
73	SEG32	3800	561
74	SEG33	3720	561
75	SEG34	3640	561
76	SEG35	3560	561
77	SEG36	3480	561
78	SEG37	3400	561
79	SEG38	3320	561
80	SEG39	3240	561
81	SEG40	3160	561
82	SEG41	3080	561
83	SEG42	3000	561
84	SEG43	2920	561
85	SEG44	2840	561
86	SEG45	2760	561
87	SEG46	2680	561
88	SEG47	2600	561
89	SEG48	2520	561
90	SEG49	2440	561
91	SEG50	2360	561
92	SEG51	2280	561
93	SEG52	2200	561
94	SEG53	2120	561
95	SEG54	2040	561
96	SEG55	1960	561
97	SEG56	1880	561
98	SEG57	1800	561
99	SEG58	1720	561
100	SEG59	1640	561
101	SEG60	1560	561
102	SEG61	1480	561
103	SEG62	1400	561
104	SEG63	1320	561
105	SEG64	1240	561
106	SEG65	1160	561
107	SEG66	1080	561
108	SEG67	1000	561
109	SEG68	920	561
110	SEG69	840	561
111	SEG70	760	561
112	SEG71	680	561
113	SEG72	600	561
114	SEG73	520	561
115	SEG74	440	561
116	SEG75	360	561
117	SEG76	280	561
118	SEG77	200	561
119	SEG78	120	561
120	SEG79	40	561
121	SEG80	–40	561
122	SEG81	–120	561
123	SEG82	–200	561
124	SEG83	–280	561
125	SEG84	–360	561
126	SEG85	–440	561
127	SEG86	–520	561
128	SEG87	–600	561
129	SEG88	–680	561
130	SEG89	–760	561

Pad No.	Pad name	X-coordinate (µm)	Y-coordinate (µm)
131	SEG90	–840	561
132	SEG91	–920	561
133	SEG92	–1000	561
134	SEG93	–1080	561
135	SEG94	–1160	561
136	SEG95	–1240	561
137	SEG96	–1320	561
138	SEG97	–1400	561
139	SEG98	–1480	561
140	SEG99	–1560	561
141	SEG100	–1640	561
142	SEG101	–1720	561
143	SEG102	–1800	561
144	SEG103	–1880	561
145	SEG104	–1960	561
146	SEG105	–2040	561
147	SEG106	–2120	561
148	SEG107	–2200	561
149	SEG108	–2280	561
150	SEG109	–2360	561
151	SEG110	–2440	561
152	SEG111	–2520	561
153	SEG112	–2600	561
154	SEG113	–2680	561
155	SEG114	–2760	561
156	SEG115	–2840	561
157	SEG116	–2920	561
158	SEG117	–3000	561
159	SEG118	–3080	561
160	SEG119	–3160	561
161	SEG120	–3240	561
162	SEG121	–3320	561
163	SEG122	–3400	561
164	SEG123	–3480	561
165	SEG124	–3560	561
166	SEG125	–3640	561
167	SEG126	–3720	561
168	SEG127	–3800	561
169	SEG128	–3880	561
170	SEG129	–3960	561
171	SEG130	–4040	561
172	SEG131	–4120	561
173	SEG132	–4200	561
174	SEG133	–4280	561
175	SEG134	–4360	561

Pad No.	Pad name	X-coordinate (µm)	Y-coordinate (µm)
176	SEG135	–4440	561
177	SEG136	–4520	561
178	SEG137	–4600	561
179	SEG138	–4680	561
180	SEG139	–4760	561
181	SEG140	–4840	561
182	SEG141	–4920	561
183	SEG142	–5000	561
184	SEG143	–5080	561
185	SEG144	–5160	561
186	SEG145	–5240	561
187	SEG146	–5320	561
188	SEG147	–5400	561
189	SEG148	–5480	561
190	SEG149	–5560	561
191	SEG150	–5640	561
192	SEG151	–5720	561
193	SEG152	–5800	561
194	SEG153	–5880	561
195	SEG154	–5960	561
196	SEG155	–6040	561
197	SEG156	–6120	561
198	SEG157	–6200	561
199	SEG158	–6280	561
200	SEG159	–6360	561
201	SEG160	–6440	561
202	NC	–6520	561
203	NC	–6600	561
204	NC	–6680	561
205	NC	–7121	360
206	NC	–7121	280
207	BLANKOUT	–7121	200
208	SEG-TESTOUT	–7121	120
209	LOADOUT	–7121	40
210	CLOCKOUT	–7121	–40
211	NC	–7121	–120
212	DATAOUT	–7121	–200
213	NC	–7121	–280
214	NC	–7121	–360

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